Remarks

Claims 1 [] are amended herein, and Claim 6 is canceled. No new matter is introduced by any of the amendments, and entry thereof is requested.

Claims 1 - 5 and 7 - 40 are in the application, of which claims 20 - 38 have been withdrawn as being directed to a nonelected invention. Accordingly, claims 1 - 5, 7 - 19, 39 and 40 are now under consideration. Reconsideration of the application, as amended, is requested.

Applicant's invention is directed to multi-package modules (MPM) including stacked first and second packages, each of which includes a die attached to a substrate, in which the first and second substrates are interconnected by wire bonding, and in which at least one of the packages includes a flip-chip ball grid array package having a flip-chip in a die-down configuration. Advantageously, according to the invention, the second package and the first package can be separately tested before assembly, so that second packages not testing as "good" can be discarded and only "good" second packages used in the finished MPM.

The points raised in the Office action will now be addressed, beginning with the objection to the claims.

Claim Objection

Claim 1 was objected to, the Examiner asserting that there was insufficient antecedent basis for the recitation "the first and second substrates" in line 2 of the claim. Applicant disagrees: the "first and second substrates" are the substrates, respectively, of the "first and second packages, each said package including a die attached to a substrate", as recited in the claim.

Claim 1 is amended herein to more fully recite the structures of the first and second packages, and this objection should be withdrawn.

Amendments to the Specification

The specification is amended herein to correct an error of a typographical or editorial nature (paragraph **[0068]**); additionally, paragraph **[0002]** is amended to update the Related Applications data.

Applicant notes particularly that related Application No. 10/632,551 (CPAC 1017-4 D2) issued January 4, 2005 as U.S. Patent No. 6,838,761; and, further, that the Issue Fee has been paid in related Application No. 10/632,550 (CPAC 1017-7 D5). Claim 6 is canceled herein in view of U.S. Patent No. 6,838,761.

Rejections under 35 U.S.C. §§ 102(b), 102(e); 103(a)

Kikuma

Claims 1 - 19 and 39 - 40 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kikuma *et al.* U.S. Patent No. 6,621,169 ("Kikuma").

Regarding claim 1, the Examiner characterized Kikuma as follows:

> Kikuma discloses a multi-package module, as shown in figs. 10, 12-17, comprising stacked first package including a first die 72 attached to a first substrate 26; and a second package including a second die 74 attached to a second substrate 76, wherein the first and second substrates 26/76 are interconnected by wire bonding 84, and wherein the first package comprise a flip-chip ball grid array package having flip chip in a die-down configuration (fig. 15B).

Regarding claim 2, the Examiner characterized Kikuma as follows:

> Kikuma discloses the multi-package module wherein the second package is a wire bonded land grid array package. See figs. 15B.

Regarding claim 2, the Examiner characterized Kikuma as follows:

> Kikuma discloses the multi-package module wherein the die and wire bonds in the second package are fully encapsulated with a molding material 40.

Applicant, respectfully, disagrees with the Examiner's reading of Kikuma and application of it to Applicant's invention. As explained below, Kikuma does not teach or suggest a multi-package module including stacked packages, as in Applicant's claimed invention.

Kikuma describes a "stacked semiconductor device" having "a plurality of semiconductor chips of desired sizes stacked as one package", constructed by serially mounting semiconductor chips and wiring boards.

The package in Kikuma Fig. 10, for example, is constructed by production process shown in Figs. 12A to 12E. According to Kikuma, the lower semiconductor chip **72** is mounted on a flexible printed wiring board **26**; then a flexible printed wiring board **76** is placed as a second substrate on a semiconductor chip **72**; then a semiconductor chip **74** is secured onto the surface of the flexible printed wiring board **76**; then (Fig. 12C) the various semiconductor chips and wiring boards are connected by wire bonds. Thereafter the semiconductor chips **72** and **74**, together with the bonding wires **82**, **84**, and **86** are encapsulated with the encapsulation resin **40**. And the package shown in Kikuma Figs. 15A and 15B has basically the same structure as that of Fig. 10, except for the lower semiconductor device **72** being mounted to the flexible printed wiring board **26** in a face-down state; the lower semiconductor chip **72** is mounted to the flexible wiring board by flip-chip bonding, and the upper semiconductor chip **74** is mounted on the lower semiconductor chip **72** via the flexible printed wiring board **76** and then is connected by wire bonding.

Thus, Kikuma expressly teaches building up a stacked semiconductor device by serially mounting semiconductor chips, and thereafter forming electrical connection of the chips by wire bonding. Kikuma does not teach or suggest a multi-package module having stacked packages in which at least the second package is encapsulated, as in Applicant's invention as claimed.

There is in Kikuma no second package, in the meaning of the term "package" as in Applicant's invention as claimed. Particularly, according to Applicant's invention the second package is constructed as a die attached to and electrically connected to a second substrate, and encapsulated with a package encapsulation. In Kikuma there is no package encapsulation protecting the electrical connections between the die **74** and the flexible wiring board **76**. The distinction is significant at least for the reason that it is not possible to test the upper chip on the flexible substrate prior to assembly of the entire device stack, while in Applicant's invention, the second package can be tested prior to stacking it upon the lower package.

Applicant's claim 1 is amended herein to recite that the second package is encapsulated with a package encapsulation; and Kikuma does not suggest, much less teach, this feature of Applicant's invention as claimed. Accordingly, the rejection of claim 1, and of claims 2 - 19, 39 and 40 depending directly of indirectly from claim 1, should be withdrawn.

Mori

Claims 1, 6 - 7, 10 - 13 and 17 - 19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mori U.S. Patent No. 5,903,049 ("Mori"); and claims 2 - 5, 8 - 9, 14 - 16 and 39 - 40 were rejected under 35 U.S.C. § 103(a) for obviousness over Mori.

Regarding claim 1, the Examiner characterized Mori as follows:

> Mori discloses a multi-package module, as shown in figs. 1, 3, comprising stacked first and second packages 6b/6a, each said package including die 1b/1a attached to a substrate 2b/2a respectively, wherein the substrates 2b/2a are interconnected by wire bonding 7, and wherein the first package 6b comprises a flip-chip ball grid array package having a flip chip in a die-down configuration.

Applicant, respectfully, disagrees with the Examiner's reading of Mori and application of it to Applicant's invention. As explained below, Mori does not teach or suggest a multi-package module including stacked packages, as in Applicant's claimed invention.

Mori decribes a "mounting substrate" (**8** in Mori Fig. 1, *e.g.*). According to Mori, semiconductor packages **6***b* and **6***a* are mounted onto the mounting substrate **8**; semiconductor packages **6***b* and **6***a* are electrically connected to each other by wire bonds connecting their respective wiring patterns; and both semiconductor package **6***a* and semiconductor package **6***b* are electrically connected to the mounting substrate **8** by wire bonds. Although Mori is silent as to second-level interconnection, Mori expressly teaches a "mounting substrate" for the module, in addition to the "element substrates" in the packages, and Mori expressly teaches mounting the packages onto and electrically interconnecting the packages to this additional mounting substrate.

There is no teaching or suggestion in Mori of a multi-package module having stacked lower and upper packages, in which the substrate of the lower package both provides for z-level interconnection between the packages in the module, and provides for second-level interconnection of the module, as in Applicant's claimed invention.

Claim 1 is amended to recite that the module further comprises second-level interconnection solder ball pads at the lower side of the lower package substrate.

These differences are significant, for a number of reasons. Generally, the cost of substrates contributes significantly to the overall cost of a package or module, and avoiding the use of an additional substrate can bring the cost the module down. Additionally, the thickness of the substrate contributes to the overall thickness of the package or module, and avoiding the use of an additional substrate can provide for a thinner module. Moreover, the footprint of the additional mounting substrate (and, concomitantly, the module footprint) as taught by Mori must necessarily be larger than the footprint of the largest one of the packages, to permit wire bonding the packages to the mounting substrate, while, according to applicant's invention, the footprint of the module can be the same as the footprint of the lower package.

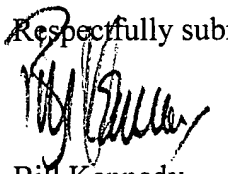
Accordingly, Mori neither teaches nor suggests Applicants' invention as claimed, and the rejection of claim 1, and of claims 2 - 5, 7 - 19, 39 and 40, depending directly or indirectly from claim 1, should now be withdrawn.

In view of the foregoing, all the claims now in the application are believed to be in condition for allowance, and action to that effect is respectfully requested.

This Response is being filed within the third month following the three months' shortened statutory period set by the Examiner for response to the Office action and, accordingly, it is accompanied by a Petition for three months' extension of time and a fee or fee authorization therefor. In the event the Examiner may determine that additional fee[s] may be required in connection with the filing of this paper, petition is hereby made therefor, and the Commissioner is authorized to charge any additional fee (or to credit any overpayment) to Deposit Account No. 50-0869 (CPAC 1017-6).

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,



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